SEMINAR NOTICE

Preston M. Green Department of Electrical and Systems Engineering

Investigating Read/Write Aggregation to Exploit Power Reduction Opportunities Using Dual Supply Voltages

MS Dissertation Defense

By

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Abstract: Power consumption plays an important role in computer system design today. On-chip memory structures such as multi-level cache make up a significant proportion of total power consumption of CPU or Application-Specific Integrated Circuit (ASIC) chip, especially for memory-intensive application, such as floating-point computation and machine learning algorithm. Therefore, there is a clear motivation to reduce power consumption of these memory structures that are mostly consisting of Static Random-Access Memory (SRAM) blocks. In this defense, I will present the framework of a novel dual-supply-voltage scheme that uses separate voltage levels for memory read and write operations. By quantitatively analyzing the cache trace for SPEC2000, Parsec, and Cortexsuite benchmarks and comparing the Read/Write sequence characterization of different computing application types, I discover that memory-intensive applications have high potential to generate long consecutive Read/Write sequences, which can be leveraged by our proposed dual-supply framework. I then perform a limit study based on ideal Read/Write re-ordering to obtain the maximum possible power saving estimate. Finally, as a case study, I apply this framework to a custom machine learning ASIC accelerator design to showcase its viability.

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DATE:	Monday, April 24, 2017
TIME:	10:00 a.m.
PLACE:	Green Hall. Room 0120

Research Advisor:
Dr. Xuan ‘Sylvia’ Zhang

This seminar is in partial fulfillment
of the Masters Degree

Washington University in St. Louis
School of Engineering & Applied Science