

# SEMINAR NOTICE

Preston M. Green Department of Electrical and Systems Engineering

## **SRAM Power Optimization Using Multiple Voltage Supplies to Exploit Read/Write Asymmetry**

MS Dissertation Defense

By

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**Abstract:** Power consumption becomes more and more critical in computer systems nowadays. Most of the previous work has been focusing on general-purpose computational core, but optimization techniques for conventional CPU core has reached a limit. Our experimental results show that read operations in SRAM can be performed at a lower supply with much reduced power consumption compared to write operations. Based on this observation and the fact that SRAM often occupies significant on-chip area of the CPU (Caches and shared SRAMs), we propose a new method to reduce the power consumption of SRAM. By dynamically switching the SRAM voltage supply between a lower voltage for read and a higher voltage for write, our method can effectively reduce SRAM power without affecting the performance of the multi-level cache hierarchy in a computer system. We can realize further power savings by lowering the supply below read voltage for hold-only operations when the SRAM is idle. Both the power switching controller implementation and the power consumption statistics from various SPEC benchmarks will be presented to demonstrate the efficiency of our proposed methods.

DATE: Friday, April 21, 2017  
TIME: 12:00 noon  
PLACE: Green Hall. Room 0120

**Research Advisor:**

Dr. Xuan 'Silvia' Zhang

This seminar is in partial fulfillment  
of the Masters Degree